

IEEE P1581

Simplifying Connectivity Tests for Complex Memories
and other Non-Boundary Scan Devices

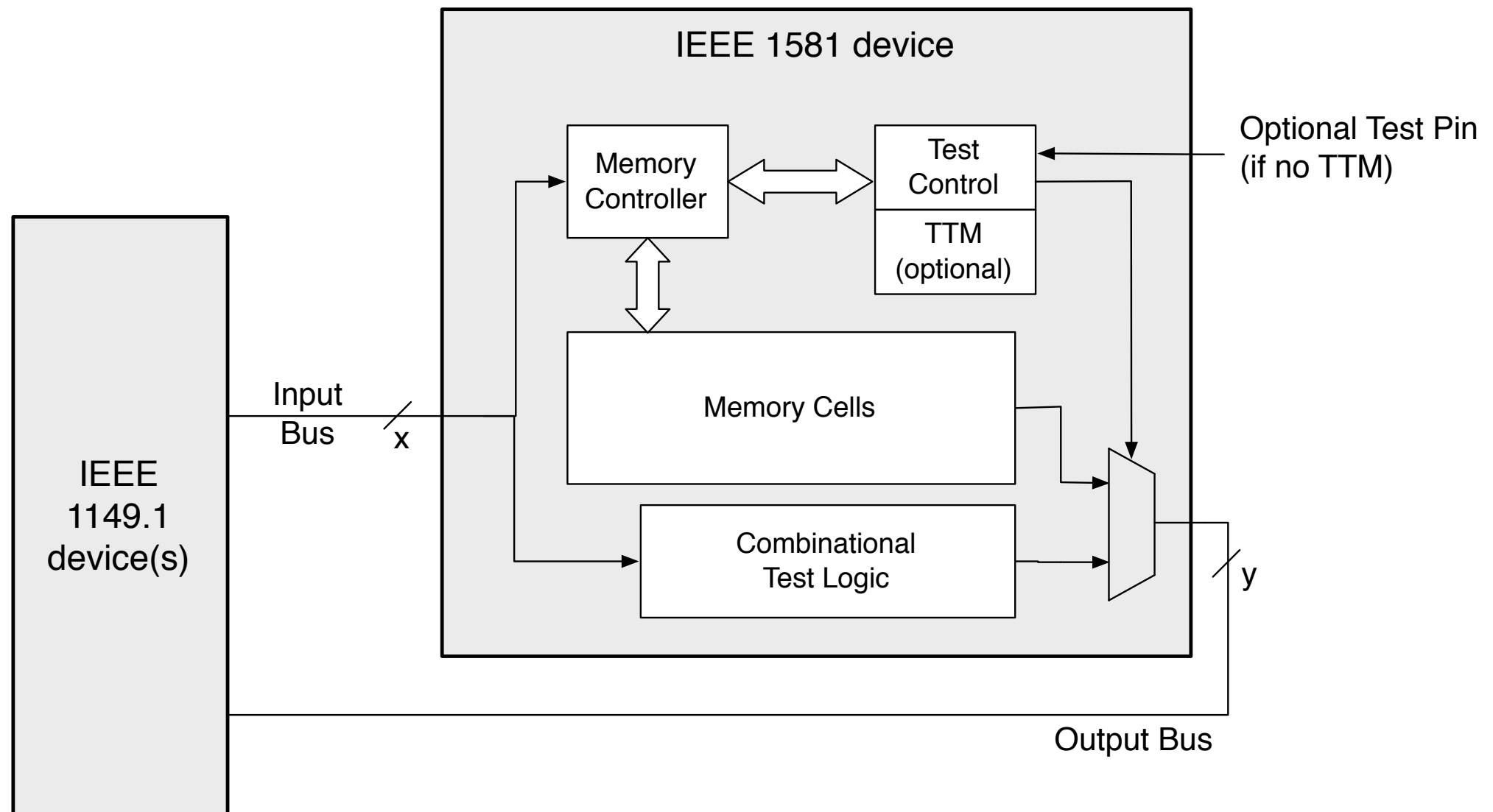
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IEEE P1581 - Introduction

- **Scope:**
Low-cost method for testing the interconnection of discrete, complex memory integrated circuits (ICs) where additional pins for testing are not available and implementing boundary scan (IEEE Std 1149.1) is not feasible;
- **Purpose:**
Improve interconnect test for discrete memory devices by specifying implementation rules for test logic and test mode entry/exit methods included in memory ICs;

Basic concept

PCB



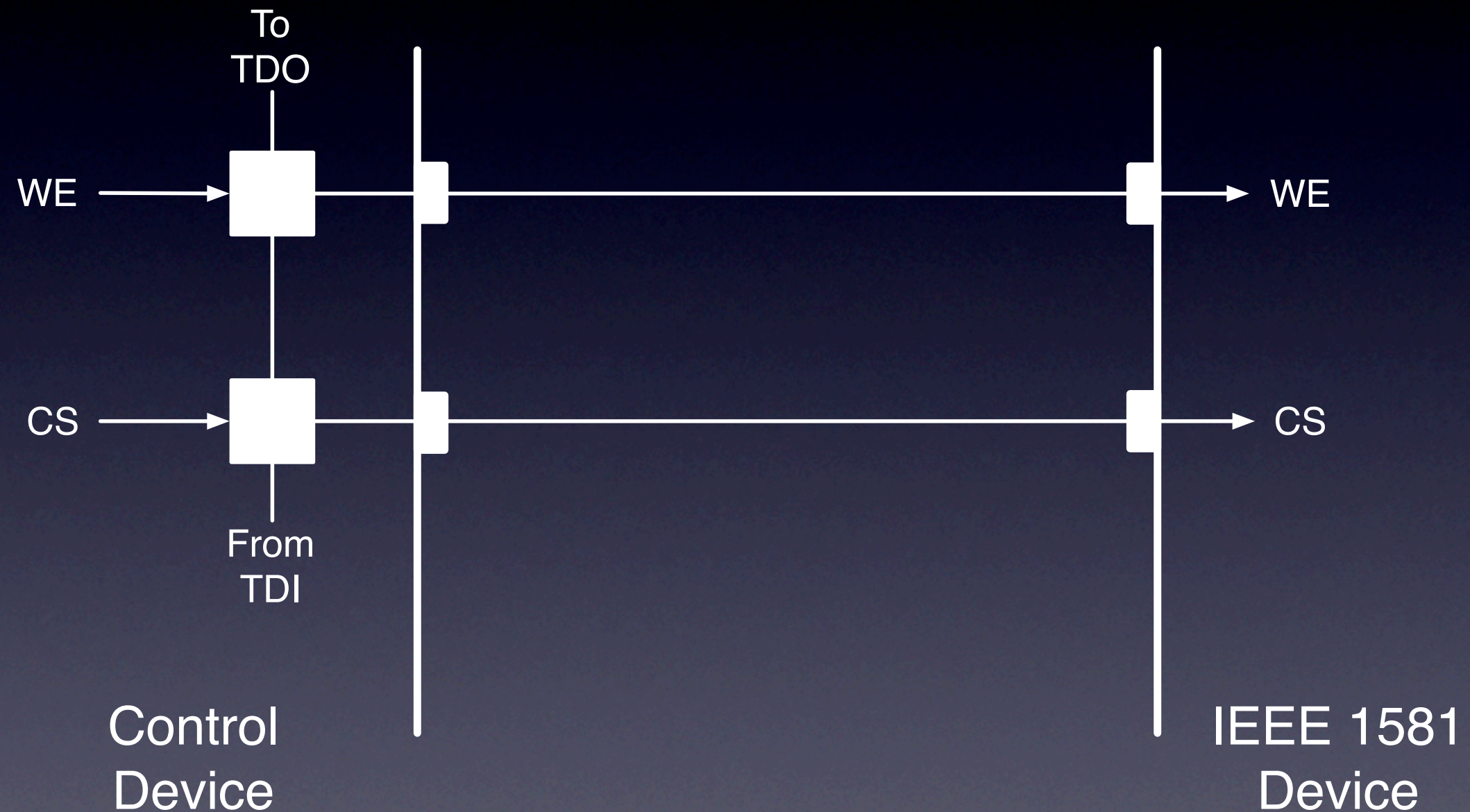
Key features

- Simple test logic implementation for memory devices (and possibly other complex, slave-type components)
- No extra pins required
- Not relying on complex memory access cycles
- Fast test execution, small test vector set
- Usable with any access methodology (Boundary scan, functional, ICT)

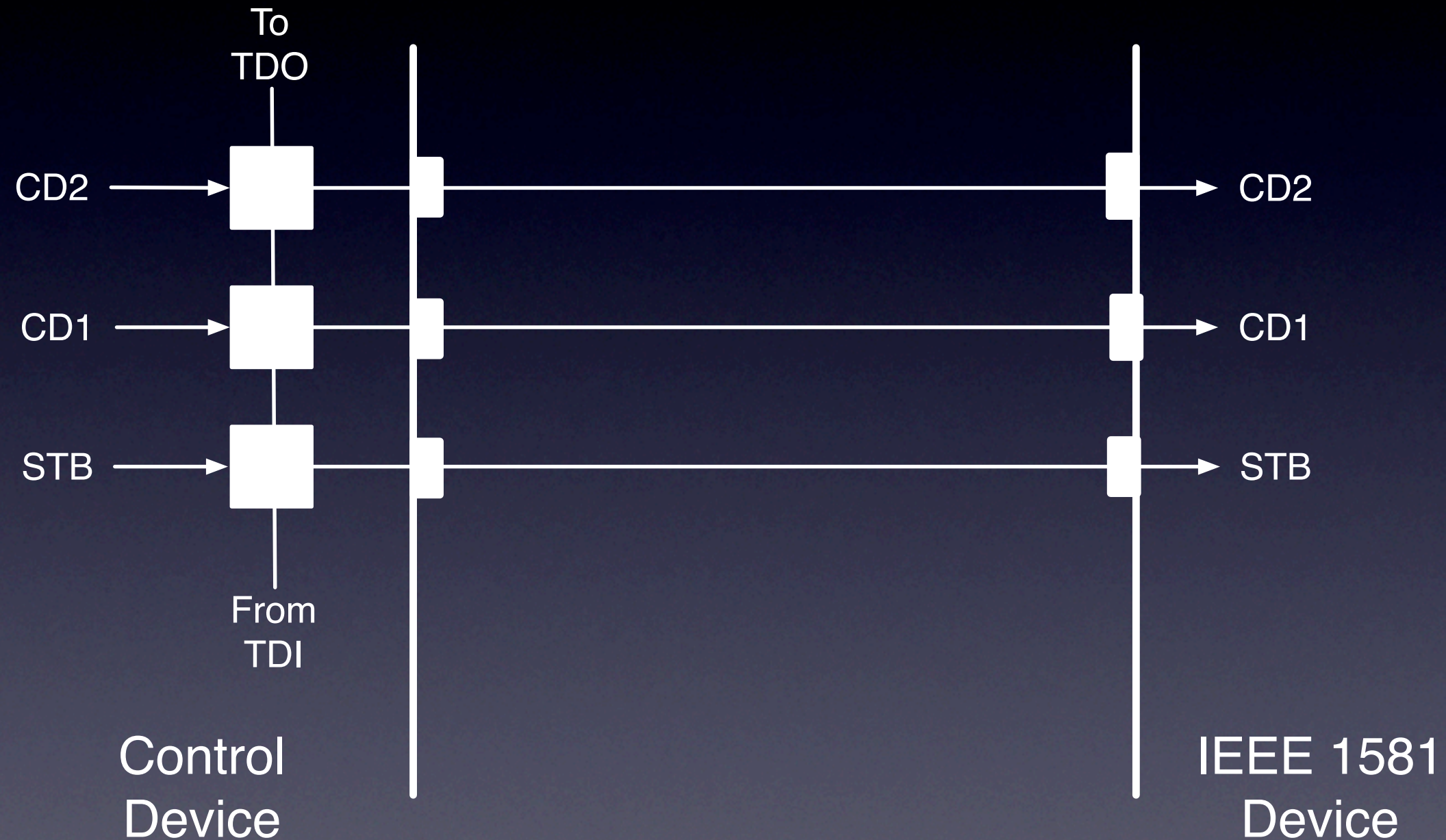
Test mode control

- Dedicated test pin (TPN), or
 - One of seven transparent test mode (TTM) control methods:
 - Non-functional stimulus (NFS)
 - Designated command codes (DCC)
 - Simultaneous input/output (SIO)
 - Clock frequency (CKF)
 - Analog level (ANL)
 - Conditional power-up initiation (CPI)
 - Default power-up initiation (DPI)
- Test entry or exit is triggered by a condition on the pins that would otherwise never exist under normal functional conditions*
- These methods require additional board-level and/or controlling device DFT to be implemented*

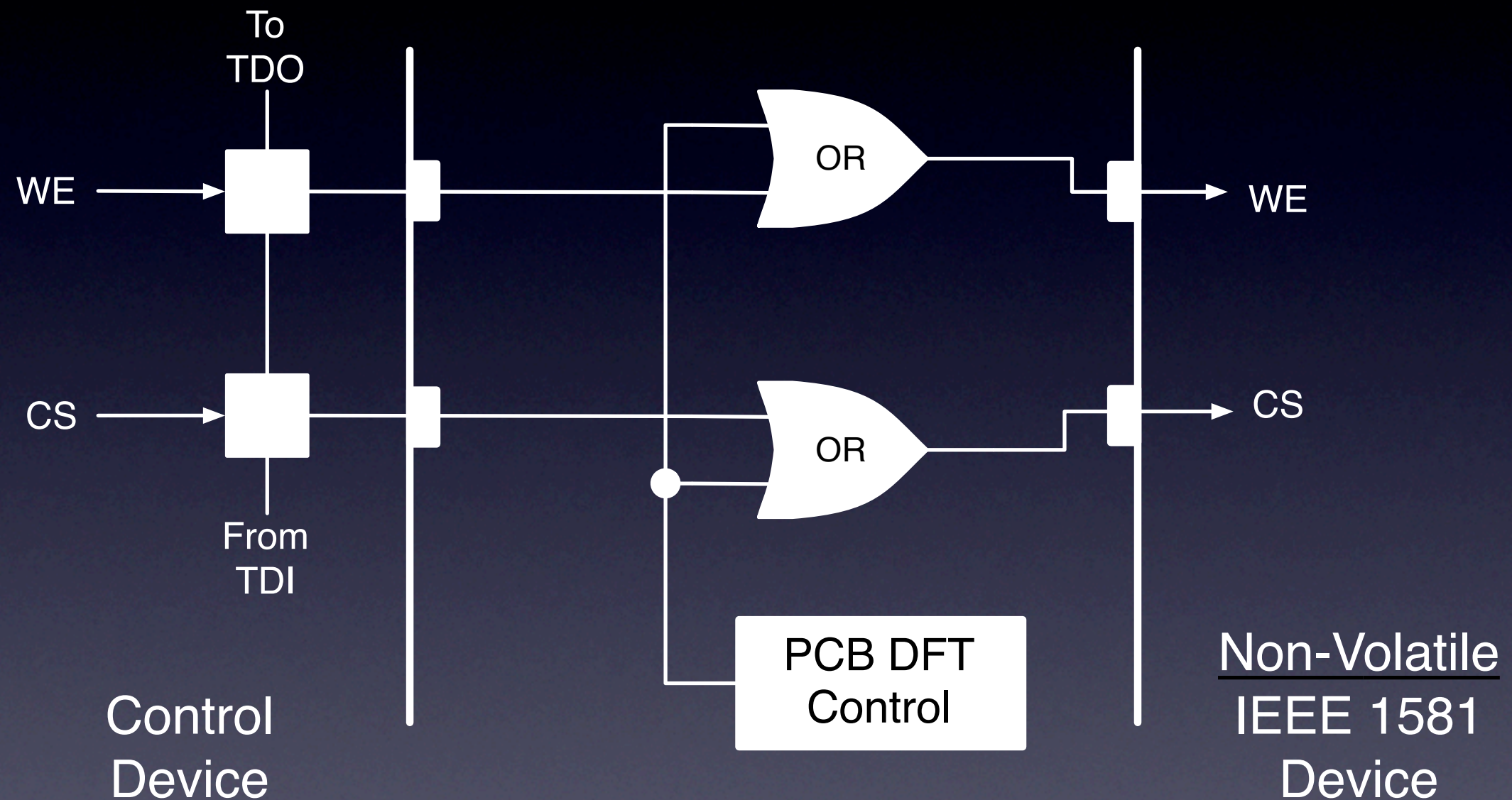
Test mode control - NFS



Test mode control - DCC



Test mode control - CPI

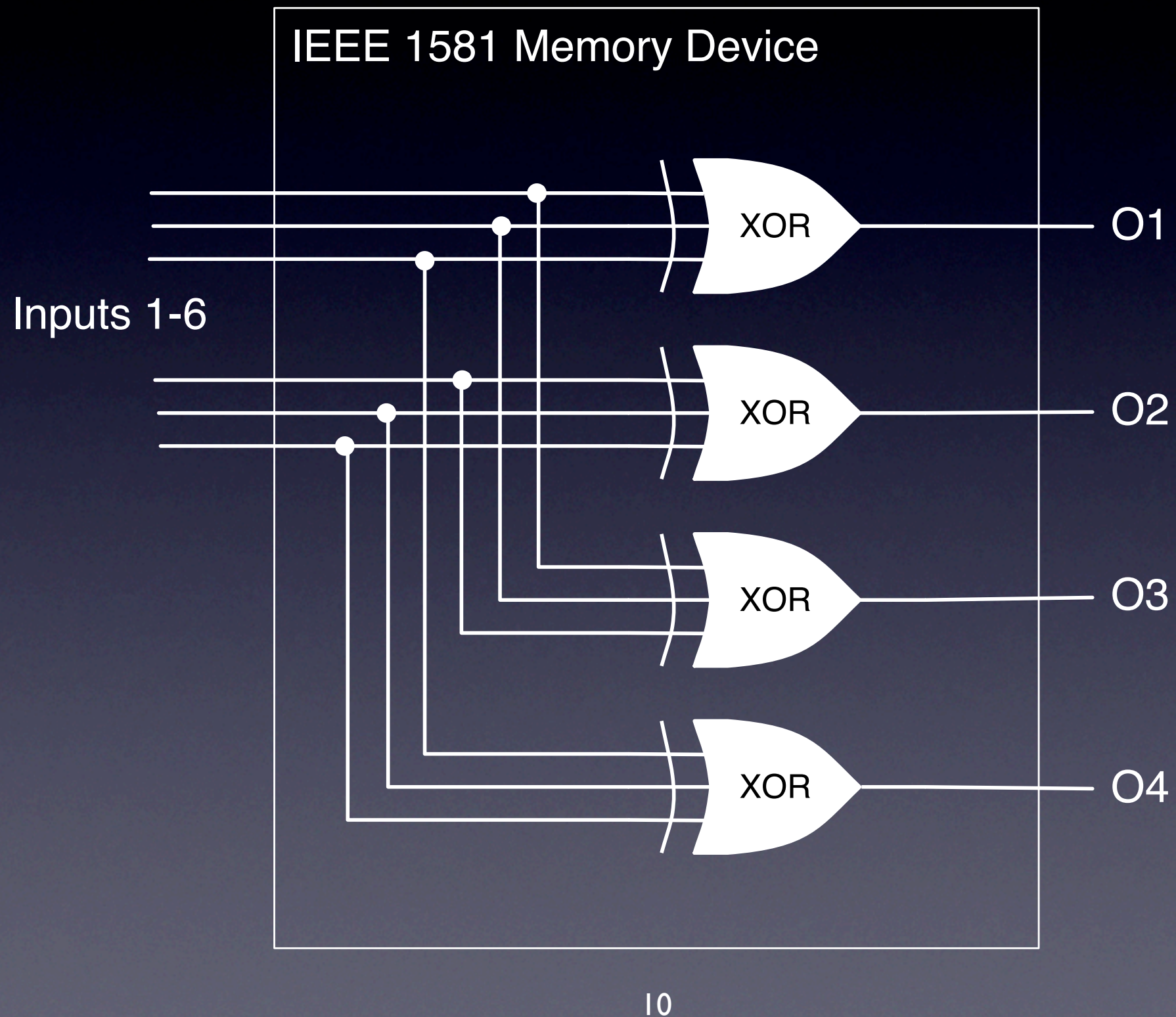


Test mode is entered if a predetermined set of logical input states exist at a predetermined period after device power-up.

Test logic

- One of three defined test logic architectures:
 - XOR (3-input XOR or XNOR gates)
 - IAX (XOR, Inverters, and AND gates)
 - XOR-2 (2-input XOR or XNOR gates)
- Or a custom test logic that satisfies rules in IEEE P1581

Test logic example - XOR



Optional test functions

- Optional test functions accessible via test pattern partitioning
- Examples include:
 - Reading a device identification (ID)
 - Control line continuity test
 - Built-in self test (BIST) access
 - Other public or private commands

Status of IEEE P1581

- Balloting completed
- Ballot group voted to accept IEEE P1581
- IEEE needs to review and finalize acceptance
- Official adoption as IEEE Std 1581 expected for mid 2010